

INFORMATION DISCLOSURE CITATION IN AN APPLICATION			ATTY. DOCKET NO. <b>57454-990</b>		SERIAL NO. <b>10/714,393</b>	
			APPLICANT <b>Hideyuki NODA, et al.</b>		FILING DATE <b>November 17, 2003</b>	
(PTO-1449)			U.S. PATENT DOCUMENTS			
EXAMINER'S INITIALS	PATENT NO.	ATE	NAME	CLASS	SUBCLASS	FILING DATE
<i>at</i>	5,101,248	3/31/1992	TAKEBUCHI	257	314	
	5,293,336	3/8/1994	Ishii et al	365	149	
	5,825,712	10/20/98	Higashi et al	365	230.03	
	4,482,985	11/13/84	Itoh et al	365	226	
	4,471,373	9/1984	Shimizu et al	257	315	
	5,610,858	3/1997	Iwahashi	365	185.23	
	5,256,892	10/93	Yoshida	257	306	
	2001/0010654	8/2001	Shau	365	222	
<i>at</i>	5,592,434	1/1997	Iwamoto et al	365	233	
FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSACTION
						YES
<i>at</i>	11-238-860	Aug. 31, 1999	JAPAN (with English abstract)	H01L	27/108	
<i>at</i>	11-214656A	8/1999	Japan (Shimizu et al)	H01L	27/108	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
<i>at</i>	"A 5.3-GB/s Embedded SDRAM Core with Slight-Boost Scheme", A. Yamazaki et al., IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 5, MAY 1999, pp. 661-667					
EXAMINER <i>at</i>	DATE CONSIDERED 06/21/2005					

**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.